ABSTRACT

A power switch, and a method, for use with a power switch having a field-effect transistor (FET) including source, drain and gate terminals. The power switch includes a first field-effect transistor (FET) having a first drain coupled to the drain terminal, a first source coupled to the source terminal, and a first gate; and, a second FET having a second drain coupled to the drain terminal, a second source coupled to the source terminal, and a second gate. The second FET has a gate length (L_G) that is greater than or less than an L_G of the first FET and has a length of a drain (L_D) that is greater than or less than an L_D of the first FET. The power switch further includes a control circuit coupled to the gate terminal, the first gate, and the second gate.